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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT UNDER 37 C.F.R. § 1.53©

INVENTOR(S)

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☐ *Additional inventors are being named on the ___ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

APPARATUS AND METHOD FOR CONTROLLING FEED-FORWARD AMPLIFIERS

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ENCLOSED APPLICATION PARTS *(check all that apply)*

[X]	Specification *Number of Pages*	14	☐	CD(s), Number	
[X]	Drawings *Number of Sheets*	1	☐	Other (specify)	
[X]	Application Data Sheet. See 37 C.F.R. § 1.76				

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT *(check one)*

☐ Applicant claims small entity status. See 37 C.F.R. § 1.27.

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The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

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☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

_____

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REGISTRATION NO. (If appropriate) 44,751

Docket Number 213222.00064

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

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PROVISIONAL APPLICATION COVER SHEET
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INVENTOR(S)/APPLICANT(S)		
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Number 2 of 4

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Form #79

APPLICATION DATA SHEET

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APPARATUS AND METHOD FOR CONTROLLING FEED-FORWARD AMPLIFIERS

FIELD OF THE INVENTION

The present invention relates to amplifiers. More specifically, the present invention relates to an apparatus and method for controlling gain and phase adjustments in a feed-forward amplifier.

BACKGROUND OF THE INVENTION

One well-known form of amplifier is the feed-forward amplifier. In order to achieve linearity in a feed-forward amplifier, careful control of the amplifier circuitry is required. In particular, in feed-forward amplifiers two or more gain and phase adjusters are often employed and the taps of each of these adjusters are carefully steered to achieve linearity through the amplifier.

Within the art of feed-forward amplifiers, it is known to use detector-controller circuits, one for each gain-and-phase adjuster. Each detector-controller circuit is operable to steer the taps of its respective gain-and-phase adjuster in the feed-forward amplifier so that the main amplifier and correctional amplifier can properly cooperate in order to reduce error introduced by the main amplifier.

Detector-controller circuits used in feed-forward amplifiers use a number of different techniques to control the phase and gain adjustments in signal and intermodulation cancellation loops. Typically, the signal cancellation loop is nulled by measuring the total power at the cancellation node and adaptively minimizing it. This makes sense because the undistorted input signal is being removed (cancelled) from the composite signal. The total power will be minimized when this cancellation is a maximum. The intermodulation cancellation loop can be nulled using a number of techniques including pilot tones, intermodulation detectors, vector signal analysis, and many others.

A first order or textbook analysis of a feed-forward amplifier would suggest that only undesired distortion products should be amplified by the correction amplifier. In practice, this turns out to be neither possible nor desirable. There will always be some residue of the original undistorted signal in the correction amplifier signal. This is because (1) signal cancellation at

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the summing node is not perfect, and (2) the main amplifier in the signal cancellation loop will characteristically be driven into non-linearity on signal peaks, resulting in loop imbalance. Perfect cancellation could only be achieved in a perfectly linear system.

Conventional wisdom has been that the signal cancellation loop should be adjusted to yield the best overall cancellation possible, given the dynamic range of the signal used. Again, this is characteristically done by minimizing the total power at the summing node, although it may be done by other techniques such as pilot tone nulling.

The correction amplifier is typically a rather large amplifier that is sized to be able to handle the peak power demands placed upon it by the correction signal. Herein lies one of the oft-mentioned disadvantages of feed-forward amplifiers versus other approaches; the wasted power and cost of the correction amplifier.

Most well-designed feed-forward amplifiers use gain and phase adjustments in series and in front of the main amplifier in the signal cancellation loop. The most important reason for doing this is to maintain constant gain of the feed-forward amplifier in the face of drift in the main amplifier caused by factors such as temperature variation and component aging. Because the loss in the delayed path in the signal cancellation loop can generally be counted upon not to vary with temperature, placing the gain adjustment in series with the amplifier, and maintaining constant signal cancellation, will result in constant gain. This is very useful from a systems point of view, although it is not, strictly speaking, necessary.

SUMMARY OF THE INVENTION

Present invention recognizes that maximal cancellation in the signal cancellation loop is not generally desirable. An apparatus and method is disclosed to optimally imbalance the signal cancellation loop so as to improve performance by using the correction amplifier to provide some incremental power to the output of the feed-forward amplifier.

With gain and phase adjusters placed in series with the main amplifier, the inventor has found that it is possible to increase the overall output power of a feed-forward amplifier by imbalancing the signal cancellation loop. Doing so will, of course, vary the main amplifier's output power and level of intermodulation generation. The question now is, how to imbalance the signal-cancellation loop to provide the optimum combination of signal and distortion

products to the correction amplifier while providing best overall performance of the feed-forward amplifier. At first glance it would appear that the gain and phase adjusters in both loops could just be adjusted to yield best performance (minimum intermodulation). However, the inventor has found that the signal cancellation loop should first be nulled using a conventional technique (minimizing total power at the summing node). There are two reasons for this. First, given no other factors, the intermodulation of the main amplifier will be minimized when the output is minimized. Therefore, from a cold start, the gain adjustment of the signal cancellation loop will be driven to minimum just to minimize intermodulation, which is not a very useful result. Second, there needs to be a minimum level of cancellation so that the signal presented to the correction amplifier does not overwhelm it and drive it into saturation.

The solution is surprisingly straight-forward. First, the signal cancellation loop should be balanced by minimizing total power at the summing node. Second, the intermodulation cancellation loop should be balanced using an intermodulation detector or other conventional means for balancing the intermodulation cancellation loop. Third, a transition should be made to balancing the signal cancellation loop using the intermodulation detector. Note that then four adjustments (gain and phase in both loops) are being made based upon one measurement (intermodulation at the output of the feed-forward amplifier). The gain adjustment in the signal cancellation loop will no longer be driven to zero to minimize the intermodulation coming from the main amplifier, because in doing so, the signal to the correction amplifier would be greatly increased, resulting in greater overall intermodulation from the feed-forward amplifier. Characteristically, the drive to the main amplifier will be reduced very slightly, yielding a component of the desired signal at the input of the correction amplifier, which, when amplified will add in phase to the signal from the main amplifier. A fine balancing act is then played out, with the main and correction amplifiers driven at optimum levels to yield maximum desired signal and minimum intermodulation at the output of the feed-forward amplifier. Some slight variation in gain of the feed-forward amplifier will result from this balancing act but it is negligible from a systems point of view.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the present invention will now be described, by way of example only, with reference to the attached Figure, wherein:

Figure 1 is a block diagram of a feed-forward amplifier in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to Figure 1, a feed-forward amplifier in accordance with an embodiment of the invention is indicated generally by reference numeral 10. The feed-forward amplifier 10 comprises an amplifier portion 12 and a detector-controller portion 14.

The amplifier portion 12 has an input port 16 and an output port 18. A main signal path runs between the input port 16 and the output port 18 and consists of a series connection of a first main path splitter 20, a main signal path gain and phase adjuster 22, a main amplifier 24, a second main path splitter 26, a main signal path delay element 28, a first main path coupler 30, and a third main path splitter 32.

While one output of first main path splitter 20 continues along the main signal path, the other output of first main path splitter 20 heads along a feed-forward path consisting of a feed-forward signal path delay element 34, a feed-forward path coupler 36, a feed-forward path splitter 38, a feed-forward signal path gain and phase adjuster 40, and a correctional amplifier 42. The output of the correctional amplifier 42 leads to an input of the second main path coupler 30. An output of the second main path splitter 26 is connected to an input of the feed-forward path coupler 36, by an attenuator 43.

The main signal path gain and phase adjuster 22 has a gain-control input tap T_1 and a phase-control input tap T_2. Similarly, the feed-forward signal path gain and phase adjuster 40 has a gain-control input tap T_3 and a phase-control input tap T_4. In each case, the gain-control input tap T_1, T_3 can be steered to control the amplitude and the phase-control input tap T_2, T_4 can be steered to control the phase of the signal passing through the respective gain and phase adjuster. As used herein, the terms "steer", "steered" and "steering" are intended to comprise all suitable methods of adjusting or controlling of the taps of a gain and phase adjuster.

Also included in the amplifier portion 12 is an intermodulation receiver 44, the input of which is connected to the third main path splitter 32.

The detector-controller portion 14 includes an SPDT switch 46, one throw of which is

connected to an output of the feed-forward path splitter 38 and the other throw of which is connected to the output of the intermodulation receiver 44. The detector-controller portion 14 also includes a signal-power detector/processor 48 and an intermodulation detector/processor 50, each detector/processor having an input and two outputs. The input of the signal-power detector/processor 48 is connected to the pole of the SPDT switch 46. The input of the intermodulation detector/processor 50 is connected to the output of the intermodulation receiver 44. It should be noted that the signal-power detector/processor 48 thereby receives either a signal from the output of the feed-forward path splitter 38 or a signal from the output of the intermodulation receiver 44, depending upon the setting of the SPDT switch 46. Further, in the present embodiment of the invention, the SPDT switch 46 is implemented in firmware in a digital signal processor. The intermodulation detector/processor 50, of course, always receives the output of the intermodulation receiver 44.

One output of the signal-power detector/processor 48 is connected to the input of a signal-power gain controller 52 and the other to the input of a signal-power phase controller 54. The output of the signal-power gain controller 52 is connected to the gain-control input tap T_1 and the output of the signal-power phase controller 54 is connected to the phase-control input tap T_2. Similarly, the outputs of the intermodulation detector/processor 50 are connected to the inputs of an intermodulation gain controller 56 and an intermodulation phase controller 58, respectively. The output of the intermodulation gain controller 56 is in turn connected to the gain-control input tap T_3 and the output of the intermodulation phase controller 58 is connected to the phase-control input tap T_4.

Those skilled in the art will recognize the feed-forward amplifier 10 differs from conventional feed-forward amplifiers primarily in the presence of the SPDT switch 46. When the SPDT switch 46 connects the signal-power detector/processor 48 to an output of the feed-forward path splitter 38, the feed-forward amplifier 10 will operate in the following conventional manner. An input signal applied to the input port 16 is split by the first main path splitter 20 into the main-signal path and the feed-forward path. The portion of the input signal proceeding down the main signal path passes through the gain and phase adjuster 22 and is then amplified by the main amplifier 24. Non-linearity in the main amplifier 24 may add distortion to the amplified signal. A portion of the signal coming out of the main amplifier 24 is split from the main signal path by the second main path splitter 26, attenuated by the attenuator 43, and coupled into the

feed-forward path by the feed-forward path coupler 36. Meanwhile, the portion of the input signal proceeding down the feed-forward path from the first main path splitter 20 has passed through the feed-forward signal path delay element 34 before entering the feed-forward path coupler 36. The delay imposed by the feed-forward signal path delay element 34 is chosen in the design of the feed-forward amplifier 10 to approximately match the delay caused by the main amplifier 24 in the main signal path. Further, the attenuation provided by the attenuator 43 is chosen so that the portion of the attenuated signal due to the input signal approximately cancels out the signal entering the feed-forward path coupler 36 from the feed-forward signal path delay element 34. Alternatively, the attenuation provided by the attenuator 43 may be provided in the second main path splitter 26, in which case attenuator 43 would not be needed. The net result is that the signal at the feed-forward path splitter 38 is predominately distortion introduced by the main amplifier 24. However, some of the input signal will generally also be present at the feed-forward path splitter 38 unless the delay imposed by the feed-forward signal path delay element 34 and the attenuation provided by the attenuator 43 are precisely correct. Even if the delay and attenuation are correctly chosen initially, the main amplifier 24 will inevitably drift due to temperature changes, aging, etc.

It is well-known to correct for such drift in the main amplifier 24 by adding a gain and phase adjuster such as the main signal path gain and phase adjuster 22 to the main signal path upstream of the main amplifier 24 so that the input signal remaining at the feed-forward path splitter 38 can be minimized. Alternatively, a gain and phase adjuster may be added in the feed-forward path upstream of the feed-forward path coupler 36 or in series or in place of the attenuator 43 to accomplish the same result. Assuming that the SPDT switch 46 is set so as to connect the feed-forward path splitter 38 to the signal-power detector/processor 48, the signal present at the feed-forward path splitter 38 is presented to the signal-power detector/processor 48. The signal-power detector/processor 48 measures the total power of the signal applied to it and instructs the signal-power gain controller 52 and the signal-power phase controller 54 to steer the gain-control input tap T_1 and the phase-control input tap T_2 so as minimize the total power measured by the signal-power detector/processor 48. The result will tend to be that the portion of the input signal present at the feed-forward path splitter 38 will be minimized. The details of how the signal-power gain controller 52 and the signal-power phase controller 54 determine how to steer the gain-control input tap T_1 and the phase-control input tap T_2 is outside

the scope of the invention; those skilled in the art will be aware of numerous algorithms for so doing.

Meanwhile, the signal at the feed-forward path splitter 38, which is predominately distortion introduced by the main amplifier 24 passes through the feed-forward signal path gain and phase adjuster 40, is amplified by the correctional amplifier 42, and is presented to an input of the second main path coupler 30. The signal from the feed-forward path will be approximately a polarity-reversed copy of the distortion introduced by the main amplifier 24 and which will approximately cancel out the distortion present in the main signal. To increase the cancellation, the third main path splitter 32 splits the main signal downstream of the second main path coupler 30 and presents a portion of that signal to the intermodulation receiver 44, which in turn provides the intermodulation distortion present in that signal to the intermodulation detector/processor 50. The intermodulation detector/processor 50 instructs the intermodulation gain controller 56 and the intermodulation phase controller 58 to steer the gain-control input tap T_3 and the phase-control input tap T_4 so as minimize the intermodulation received by the intermodulation receiver 44. The details of how the intermodulation gain controller 56 and the intermodulation phase controller 58 determine how to steer the gain-control input tap T_3 and the phase-control input tap T_4 is outside the scope of the invention; those skilled in the art will be aware of numerous algorithms for so doing.

The operation of the feed-forward amplifier 10 as described above (assuming the SPDT switch 46 is set so as to connect the feed-forward path splitter 38 to the signal-power detector/processor 48) is conventional. However, the inventor has found that by operating the feed-forward amplifier 10 in the following unconventional manner significantly greater overall gain can be achieved. First, the feed-forward amplifier 10 should be powered up. The total power measured by the signal-power detector/processor 48 and the intermodulation distortion measured by the intermodulation detector/processor 50 should be minimized in the conventional manner as described above. However, the SPDT switch 46 should then operated to connect intermodulation receiver 44 to the signal-power detector/processor 48. From then on the signal-power detector/processor 48 will instruct the signal-power gain controller 52 and a signal-power phase controller 54 to steer the gain-control input tap T_1 and the phase-control input tap T_2 so as minimize the intermodulation received by the intermodulation receiver 44 rather than total power at feed-forward path splitter 38. It should be noted that the intermodulation

detector/processor 50 will simultaneously be instructing the intermodulation gain controller 56 and the intermodulation phase controller 58 to steer the gain-control input tap T_3 and the phase-control input tap T_4 so as minimize the intermodulation received by the intermodulation receiver 44.

The inventor has found that it is advisable to reduce how fast the controllers 52, 54, 56, 58 attempt to null the loops in order to maintain stability after the SPDT switch 46 has been switched so as to route the output of the intermodulation receiver 44 to the signal-power detector/processor 48. Conventionally, the algorithms used in the controllers 52, 54, 56, 58 include step sizes for changes to gain or phase. The inventor suggests that the step sizes used by the gain controllers 52, 56 and the signal-power phase controllers 54, 58 in varying the settings of the gain-control input taps T_1, T_3 and the phase-control input tap T_2, T_4 be reduced after the SPDT switch 46 has been switched.

The end result of applying to invention to the feed forward amplifier 10 should be that complete input signal cancellation does not take place at the feed-forward path splitter 38 and the gain of the main amplifier 24 should be reduced slightly, causing the portion of the input signal present at the feed-forward path splitter 38 to be less than the feed-forward signal coming from the feed-forward signal path delay element 34. As a result a portion of the signal presented to the input port 16 should enter the correctional amplifier 42, and be amplified and added in phase to the main path signal at the first main path coupler 30.

The invention has been applied to the feed-forward amplifier disclosed in the inventor's co-pending United States Patent Application Serial No. 10/016,691, filed December 17, 2001, which is hereby incorporated by reference in its entirety. The block diagram of the feed-forward amplifier disclosed in that application is identical to Figure 1 herein if the SPDT switch 46 and the connection from the intermodulation receiver 44 to one throw of the SPDT switch 46 are removed from Figure 1 (and an output of the feed-forward path splitter 38 is connected directly to the signal-power detector/processor 48). Hence the modifications needed to apply the invention to the feed-forward amplifier disclosed in that application are identical to those described above for a conventional feed-forward amplifier. The operations that take place in the detector-controller portion of the feed-forward amplifier disclosed in co-pending United States Patent Application Serial No. 10/016,691 are unconventional, but also minimize power at the

signal-cancellation node and intermodulation at the output of the amplifier. The inventor believes that it is reasonable to expect a similar or the same improvement to a conventional feed-forward amplifier as that obtaining in modifying the feed-forward amplifier disclosed in co-pending United States Patent Application Serial No. 10/016,691 in accordance with the invention Those results are that modifying the feed-forward amplifier disclosed in co-pending United States Patent Application Serial No. 10/016,691 provided approximately 1 dB higher output power for the same intermodulation distortion. In addition to higher output power, efficiency was improved. Those skilled in the art will recognize that these results are remarkable, given the lengths to which one must go to get tenths of a dB, and the cost of providing those tenths of a dB.

Those skilled in the art of feed-forward amplifier design will also understand that the invention should be applicable to increase the overall gain of other feed-forward amplifiers, such as those that use a pilot tone or other performance measuring means for nulling the signal and intermodulation-cancellation loops.

The above-described embodiments of the invention are intended to be examples of the present invention and alterations and modifications may be effected thereto by those of skill in the art without departing from the scope of the invention that is defined solely by the claims appended hereto.

Claims:

1. A feed-forward amplifier, comprising a signal cancellation loop and a intermodulation cancellation loop, the feed-forward amplifier configured to operate so that on start-up the signal cancellation loop is balanced so as to minimize signal power in the feed-forward path and then is unbalanced and operated so as to minimize intermodulation at the output of the feed-forward amplifier.

2. A feed-forward amplifier, comprising:

an input port 16;

an output port 18;

a first main path splitter 20, the input of which is connected to the input port 16 so that when an input signal applied to the input port 16 it is split by the first main path splitter 20 into a main signal and a feed-forward signal;

a main signal path gain and phase adjuster 22, the input of which is connected to the first output of the first main path splitter 20, the main signal path gain and phase adjuster 22 having a gain-control input tap T_1 and a phase-control input tap T_2 configured so that the voltage levels on the taps control the gain and phase of the main signal;

a main amplifier 24, the input of which is connected to the output of the main signal path gain and phase adjuster 22;

a second main path splitter 26, the input of which is connected to the output of the main amplifier 24;

a main signal path delay element 28, the input of which is connected to the first output of the second main path splitter 26,

a first main path coupler 30, the first input of which is connected to the output of the main signal path delay element 28;

a third main path splitter 32, the input of which is connected to the output of the first main path coupler 30 and the first output of which is connected to the output port 18;

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an intermodulation receiver 44, the input of which is connected to the second output of the third main path splitter 32,

a feed-forward signal path delay element 34, the input of which is connected to the second output of the first main path splitter 20, the delay imposed by the feed-forward signal path delay element 34 selected to approximately match the delay in the main signal caused by the main amplifier 24;

a feed-forward path coupler 36, the first input of which is connected to the output of the feed-forward signal path delay element 34;

an attenuator 43 connecting the second output of the second main path splitter 26 to the second input of the feed-forward path coupler 36, the attenuation selected so that the undistorted portion of the main signal provided to the feed-forward path coupler 36 is approximately cancelled out by the feed-forward signal;

a feed-forward path splitter 38, the input of which is connected to the output of the feed-forward path coupler 36;

an SPDT switch 46, the first throw of which is connected to the second output of the feed-forward path splitter 38 and the second throw of which is connected to the output of the intermodulation receiver 44;

a signal-power detector/processor 48, the input of which is connected to the pole of the SPDT switch 46, the signal-power detector/processor 48 configured to extract and process data from the signal presented to its input indicating how to steer the gain-control input tap T_1 and the phase-control input tap T_2 to minimize the signal presented to its input;

a signal-power gain controller 52, the input of which is connected to the first output of the signal-power detector/processor 48, the signal-power gain controller 52 configured to steer the gain-control input tap T_1 in response to data provided by the signal-power detector/processor 48 to minimize signal power at the feed-forward path splitter 38 when the SPDT switch 46 is set to connect the input of the signal-power detector/processor 48 to the second output of the feed-forward path splitter 38 and to minimize the

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intermodulation received by the intermodulation receiver 44 when the SPDT switch 46 is set to connect the input of the signal-power detector/processor 48 to the output of the intermodulation receiver 44;

a signal-power phase controller 54, the input of which is connected to the second output of the signal-power detector/processor 48, the signal-power phase controller 54 configured to steer the phase-control input tap T_2 in response to data provided by the signal-power detector/processor 48 to minimize signal power at the feed-forward path splitter 38 when the SPDT switch 46 is set to connect the input of the signal-power detector/processor 48 to the second output of the feed-forward path splitter 38 and to minimize the intermodulation received by the intermodulation receiver 44 when the SPDT switch 46 is set to connect the input of the signal-power detector/processor 48 to the output of the intermodulation receiver 44;

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a feed-forward signal path gain and phase adjuster 40, the input of which is connected to the first output of the feed-forward path splitter 38, the feed-forward signal path gain and phase adjuster 40 having a gain-control input tap T_3 and a phase-control input tap T_4;

a correctional amplifier 42, the input of which is connected to the output of the feed-forward signal path gain and phase adjuster 40 and the output of which is connected to the second input of the first main path coupler 30, the main signal path delay element 28 having a delay approximately equal to the delay in the correctional amplifier 42;

an intermodulation detector/processor 50, the input of which is connected to the output of the intermodulation receiver 44. the intermodulation detector/processor 50 configured to extract and process data from the signal presented to its input indicating how to steer the gain-control input tap T_3 and the phase-control input tap T_4 to minimize the signal presented to its input;

an intermodulation gain controller 56, the input of which is connected to the first output of the intermodulation detector/processor 50 and which steers the gain-control input tap T_3 in response to data provided the intermodulation detector/processor 50 to minimize intermodulation received by the intermodulation receiver 44; and

an intermodulation phase controller 58, the input of which is connected to the first output

of the intermodulation detector/processor 50 and which steers the phase-control input tap T_4 in response to data provided the intermodulation detector/processor 50 to minimize intermodulation received by the intermodulation receiver 44,

wherein, upon startup of the feed-forward amplifier 10, the SPDT switch 46 is set so as to connect the feed-forward path splitter 38 to the signal-power detector/processor 48 until the total power in the feed-forward path is minimized and the intermodulation received by the intermodulation receiver 44 is minimized, and then set so as to connect the intermodulation receiver 44 to the signal-power detector/processor 48.

3. A method for operating a feed-forward amplifier having a signal cancellation loop and a intermodulation cancellation loop, comprising:

on startup, operating the feed-forward amplifier so that the signal cancellation loop is balanced so as to minimize signal power in the feed-forward path; and

then, unbalanced so as to minimize intermodulation at the output of the feed-forward amplifier.

4. A method for operating a feed-forward amplifier having a signal cancellation loop including a first gain and phase adjuster, a main amplifier forming a portion of a main signal path, and a feed-forward signal path output for providing a feed-forward signal, and an intermodulation cancellation loop connected to the feed-forward signal path output, including a second gain and phase adjuster, a correctional amplifier, and a correctional coupler for coupling the output of the correctional amplifier to the main signal path downstream of the main amplifier, comprising:

steering the first gain and phase adjuster so as to minimize signal power at the feed-forward signal path output and the second gain and phase adjuster so as to minimize intermodulation downstream of the coupler;

and then, when the signal power at the feed-forward signal path output and the intermodulation downstream of the correctional coupler reach minimums,

steering both of the gain and phase adjusters so as to minimize the intermodulation downstream of the correctional coupler.

ABSTRACT

An apparatus and method for operating a feed-forward amplifier in which, after the signal-cancellation and intermodulation-cancellation loops have initially been nulled, the feed-forward amplifier is operated so that both loops are controlled so as to minimize intermodulation at the output of the feed-forward amplifier.

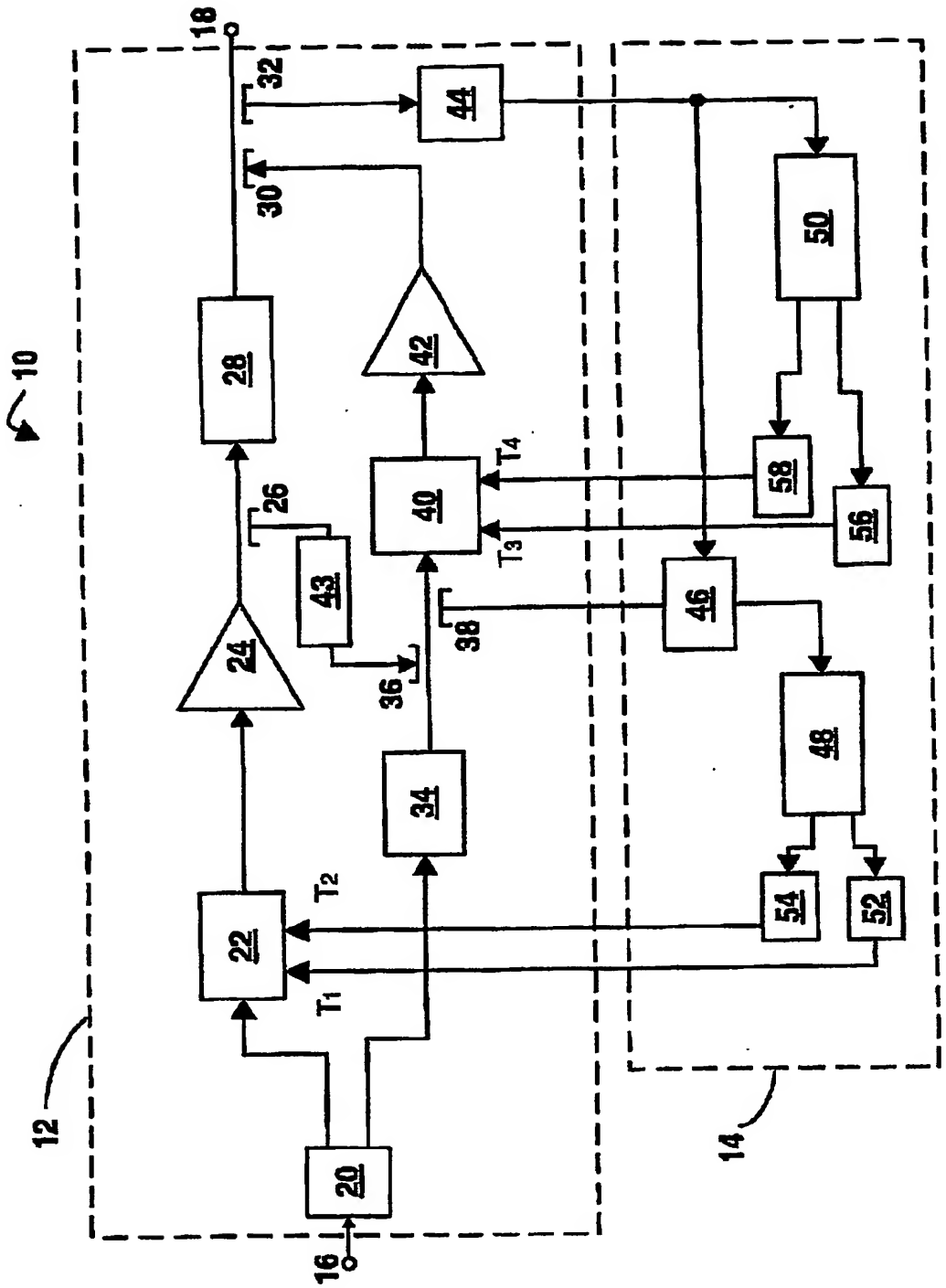
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Figure 1

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